CTB-DSM Algorithm With Topology Trigger

This is the version for 2004. No MIP conversation. If the dead time (R0 of CTB_CB001_015) is set to zero, the CTB tree is exactly the 'standard' tree
Where the CTB sum is a straight adc sum of all channels and the led bit is propagated.
In addition to the 'standard' features, the dead time (killer bit) and the topology trigger can be switched on.

CTB_CB001-015 (layer 0)
THIS Module uses one RHIC clock override cycle, input ⇒ n+2 output

Input:
- 15x 8 bit ADC values (corresponds to 15 slats)
- Least significant bit is the timing bit (bit 0/8)
- Channel 16-bit8 = LED bit

Registers:
- R0: (4bits) CTB dead time in RHIC counts
- R1/R2 (12 bits) Min/Max of ADC sum for topology bits
- R3/R4 (4bits) Min/Max for Slat sum for topology bits
- R5-R12 dummies for halt counter
- R13-R15 hidden halt counter registers

Tasks:
- Gate ADC channels with dead time
  Dead time: ADC=0 for R0*RHIC crossings after an ADC value was above zero
- Sum gated ADC's
- Count # of hit slats (gated ADC>0)
- Check out-of-time signal for hit slats
- Place thresholds on ADC sum and Slat Sum
- Build topology information
- Contains halt counter mechanics

1st Clock
- Latch in ADC values
- Latch in Led bit
- Latch timing bits (least significant bits of inputs)
- Latch and invert board mode for halt counter

2nd Clock
- Gate input channels with the dead time bit, determined from previous crossings
- Delay timing bits to sync with gated ADC's
- Delay Led Bit until clock 7

3rd Clock
- Intermediate ADC sums
- Intermediate sum of hit slats (ADC>0 after dead time gate)
- Build out-of-time bit (‘1’ if in any channel ADC>0 and bit 0=0)

4th Clock
- Total ADC sum
- Total Sum of Slats
- Delay timing bit until clock7.
- Component ‘engine dead’ determined dead time status of each channel for next crossing

5th Clock
- Delay ADC sum until clock 7
- Delay sum of slats until clck 7
- Place thresholds on ADC sum and Slat sum

6th Clock
- Combine threshold bits to topology bit + overflow

7th Clock
- Map output

8th Clock
- Latch output

Output (16 bit)
- (0-11) Sum ADC (15*8 bits)
- (12) Out-of-Time // (1: o-o-hit occurred, 0 event ok)
- (13) Topology
- (14) Topology Overflow
- (15) Gain monitoring LED fired. (see below)

Layer 1 (East, West)

Tasks:

- Sum ADC's
- Or and propagate led bit, out of time bit, topology overflow
- Propagate topology bits

Input:
8 * 16 bit from layer 0 DSM's
(0-11) ADC sum, (12) out-of-time, (13) topology), (14) topology overflow (15) led bit
8 DSM boards (pixels) per spectrometer half
// Numbers correspond to VME slots
// West: 6/7 South, 8/9 Bottom, 10/11 North, 12/13 Top
// East: 21/21 South, 18/19 Bottom, 16/17 North, 14/15

1st Clock:

- Latch adc sums (0-11)
- Latch out_of_time bit (12)
- Latch topology bits
- Latch topology overflow (14)
- Latch led bit (15)

2nd Clock

- Intermediate ADC sum
- Or led bits
- Or out_of_time bit
- Delay topology bits for 2 cycles
- Or topology overflow bits

3rd clock

- Final ADC sum
- Delay led bit
- Delay out_of_time
- Delay topology-overflow

4th clock

- Map output

Output: (32 bits):

- (0-14) ADC sum // 8*12 bits = 15 bits
- (15) led bit
- (16) out-of-time bit
- (17-22) '000000'
- (23-30) topology bits
- (31) topology overflow

Layer 2 (CTB)

Task:
- Sum ADC East and West
- Provide decision on topology
- Provide out of time signal
- 'or' all LED bits

Input: 32 bits for East and West
ADC sum (0-14), led-bit(15), out-of time (16), topology (23-30), topology overflow(31)

Registers:
- R0 (bits) topology selection
  - Bit 1=1 'veto out-of-time' hits
  - Bit 2=1 'veto topology overflow
  - Bit 3=1 'use UPC algorithm for topology decision

The default setting is R0=0x7 ('111')

1st Clock
- Latch Inputs

2nd Clock
- ADC sum
- Or led bits
- Or out-of-time bits
- Build topology bit
- Or topology overflow bit

3rd Clock
- Delay ADC sum
- Delay led bit
- Gate out-of-time bit, topology-bit and topology overflow bit with reg0

4th Clock
- Latch output

Output:
- (0-15) 16 bit ADC sum
- (30) topology bit
- (31) LED bit

Build topology decision:

1) Presently implemented UPC trigger:

If there is any hit in a top or bottom pixel the event is vetoed. Only certain South-North combinations are allowed corresponding to 2-and 4-prog events. An 'XOR' (!) is build of the two pixels '0' = eta 0-0.5 and '1' = eta 0.5-1.0 in each quadrant in east and west.

Topology bits	UPC topology = 1for the following combinations of topology bits				
East					
T-0 or T-2 -> set veto					
B-0 or B-1 -> set veto					
S-0 xor S-2	1	0	1	0	1
N-0xor N-2	1	0	0	1	1
West					
N-0 xor N-2	0	1	1	0	1
S-0 xor S-2	0	1	0	1	1
B-0 or B-2 -> set veto					
T-0 or T-2 -> set veto					